Ground Plane Influence on UTBB SOI MOSFET Short-Channel Devices

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***Abstract*— In this paper the effect of ground plane (GP) on UTBB (Ultra-Thin Body and Buried oxide) SOI (Silicon-On-Insulator) MOSFET is analyzed for short channel devices experimentally. The UTBB technology studied in this work was designed for devices down to 70nm of transistor channel length (L). This work is going to study the transistor channel length from 70nm down to 25nm, where the short channel effect (SCE) is not negligible. The parameters analyzed are threshold voltage (V_T), subthreshold swing (SS) and drain-induced barrier lowering (DIBL). The presence of GP increases V_T but no SCE is observed. The SS and DIBL present an expected SCE but only DIBL is clearly degraded by Ground Plane. The results is going to be discussed in this paper.**

Keywords — UTBB, ground plane, substrate effect, V_T, SS, DIBL

I. INTRODUCTION

The MOSFET structure (Metal Oxide Semiconductor Field Effect Transistor) has allowed the miniaturization of the integrated circuits. This implies in an electronic revolution never seen before, bringing both more and better devices each time more accessible, as well as forms of economy and human interactions never seen before in the human history.

All the transistor miniaturization, however, presents an undesirable effect called short channel effect (SCE) which degrades the device performance [1], such as the reduction of gate to channel electrostatic coupling.

New technologies of MOSFET have emerged to reduce such effects and proceed the miniaturization process, as the SOI MOSFET (Silicon on Insulator MOSFET), the FinFET (Fin Field Effect Transistor), among others. They have allowed even better control of SCE, although not being immune to these effects.

One of the emerging technologies is UTBB (Ultra-Thin Body and Buried oxide) SOI, where the silicon film and buried oxide is very thin and the gate to channel coupling is much better, decreasing the SCE, but the substrate potential influence is larger. In order to alleviate the influence of substrate potential, a ground plane implantation at buried oxide/substrate is usually done.

In that context, this research seeks to study the consequences of the use of ground plane over the threshold voltage and the short channel effects in a UTBB SOI MOSFET (Ultra-Thin Body and Buried Oxide SOI MOSFET) device with channel lengths (L) between 70nm down to 25nm, verifying the positives and negatives results on the transistor operation. It is a sequence of other previous work on the area [4] for longer L upper than 70nm.

II. DEVICE DESCRIPTION

To extract the analyzed parameters, a series of transistors UTBB SOI MOSFET (Ultra-Thin Body and Buried Oxide SOI MOSFET) with silicon thickness t_{si} = 6nm; gate oxide thickness t_{oxf} = 5nm of High-k dielectric; titanium nitrite (TiN) as the gate metal; buried oxide thickness t_{oxb} = 18nm; device's width W = 1μm were used. The channel length (L) values used were 25nm, 35nm, 45nm, 50nm, 60nm and 70nm.

The measured chips are present in the same silicon wafer of SOI technology and were built by the Interuniversity Microelectronics Centre – Imec, in Leuven, Belgium. This silicon wafer has some chips with same layout containing devices and small circuits to study the technology. To this paper, it was used two sequences of UTBB transistors in three different chips (the characteristics are the described above): one with ground plane and other without it. The channel length used were the cited above, but the sequences started in 25nm and ended in 70nm, with an increment of 5nm for each device. Although each device had its own drain, source and gate connector, the back gate connector was shared between them.

III. SUBSTRATE EFFECT MODEL

SOI MOSFET devices with thin buried oxide thickness and body silicon thickness are called UTBB [4]. In these dimensions, the third interface (buried oxide/back gate) starts to exert effects on the devices due to the potential drop at substrate and the applied back gate voltage, being expressed by a term of potential Φsub [5].

$$\Phi_{SUB} = \left[\frac{-\sqrt{2qNa_{SUB}\varepsilon_{Si}}}{2C_{ox2}} + \sqrt{\left(\frac{2qNa_{SUB}\varepsilon_{Si}}{4(C_{ox2})^2} - V_{FB3}\right) + (\Phi_{S2} - V_{GB})}\right]^2 \quad (1)$$

Where q is the electron charge, Na_{SUB} is the doping concentration on the third interface, ε_{Si} is the silicon permittivity, C_{ox2} is the capacitance of the buried oxide and Φ_{S2} is the potential of the silicon body in the interaction with the buried oxide and V_{GB} is the back gate voltage.

The drop on the potential applied on the back gate then include this additional term that, by its turn, varies with the applied tension as well.

$$V_{GB} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} + \frac{qNat_S}{2C_{ox2}} + \left(\frac{\varepsilon_{Si}}{t_S C_{ox2}} + 1\right)\Phi_{S2} - \frac{\varepsilon_{Si}}{t_S C_{ox2}}\Phi_{S1} - \Phi_{SUB} \quad (2)$$

Where Φ_{MS2} is the work function between the substrate (back gate) and silicon channel, Q_{ox2} is the charge in the buried oxide Na is the doping concentration, t_S is the silicon body thickness and Φ_{S1} is the potential of the silicon body in the interaction with the gate oxide.

$$\Phi_{SUB} = 0 \rightarrow V_{GB} \geq V_{GBmax} = \Phi_{S2} - V_{FB3} \quad (3)$$

This situation is the third interface in accumulation.

$$\Phi_{SUB} = 2\Phi_F \rightarrow V_{GB} \geq V_{GBmin} = \Phi_{S2} - V_{T3} \quad (4)$$

This situation is the third interface in inversion.

V_{T3} is the threshold voltage and V_{FB3} is the flat band voltage. Both are from the third interface.

$$V_{FB3} = \Phi_{MS3} - \frac{Q_{ox3}}{C_{ox2}} = \frac{kT}{q} ln\left(\frac{Na}{Na_{SUB}}\right) - \frac{Q_{ox3}}{C_{ox2}} \quad (5)$$

$$V_{T3} = V_{FB3} + 2\Phi_F + \frac{\sqrt{2qNa_{SUB}\varepsilon_{Si}2\Phi_F}}{C_{ox2}} \quad (6)$$

IV. RESULTS AND DISCUSSIONS

To the device studied, experimental measures of drain current I_D as a function of the gate voltage V_G were taken by the measures system Agilent B1500.

The V_G varied from 0 to 2V in steps of 10mV for four different back gate voltage values, this being V_{GB} = -3V, -1V, 0V and 1V. The measures were taken in the triode with drain to source voltage V_{DS} = 50mV and in saturation with V_{DS} = 1V. From those measures, the threshold voltage (V_T), the subthreshold swing (SS) and the drain-induced barrier lowering (DIBL) were obtained in ambient temperature.

Figures 1 and 2 show the drain currents in function of the gate voltage in triode for different values of channel length, in linear and log scale. Figure 3 shows the I_D x V_G for saturation region.

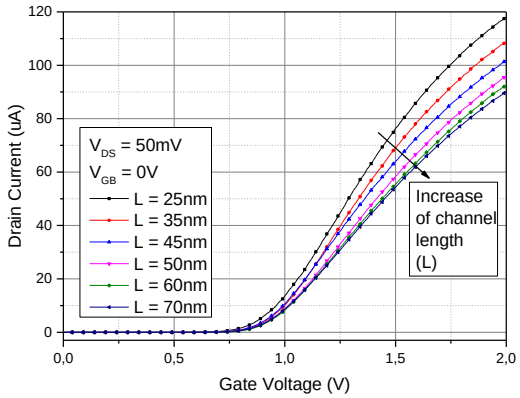

Fig. 1. Drain current as a function of gate voltage for back gate voltage V_{GB} = 0 V and V_{DS} = 50mV for different channel lengths in linear scale.

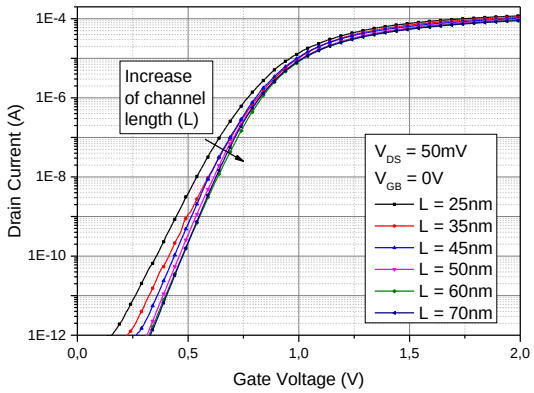

Fig. 2. Drain current as a function of gate voltage for back gate voltage V_{GB} = 0V and V_{DS} = 50mV for different channel lengths in log scale.

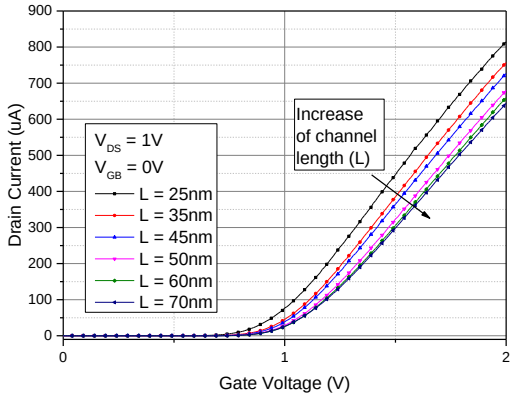

Fig. 3. Drain current as a function of gate voltage for back gate voltage V_{GB} = 0V and V_{DS} = 1V (saturation region) for different channel lengths in linear scale.

A. *Threshold Voltage - V_T*

From the drain current (I_D), the threshold voltage values were obtained by the second derivate method [6]. For that, it was used a FFT of five points smooth filter on the current curve and then a first derivative was applied; once more, the filter was used and, lastly, the curve was derivative again to obtain the d^2gm/dV_G^2 curve.

Figure 4 shows the threshold voltage as function of channel length with V_{GB} =0V and V_{DS} = 50mV for two cases: device with ground plane and device without it.

Figure 5 shows the threshold voltage as a function of the back gate voltage with L = 25nm and V_{DS} = 50mV for two situations: device with ground plane and device without it.

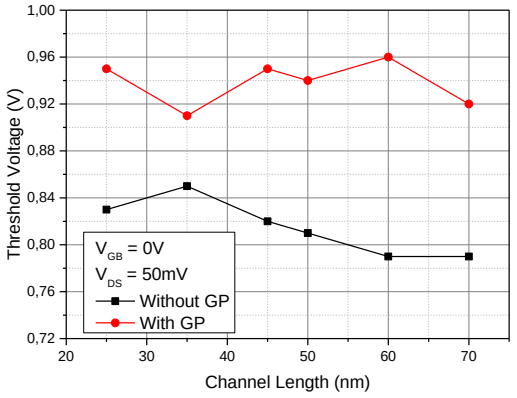

Fig. 4. Threshold voltage (V_T) as function of channel length (L) for V_{DS} = 50mV and V_{GB} = 0V.

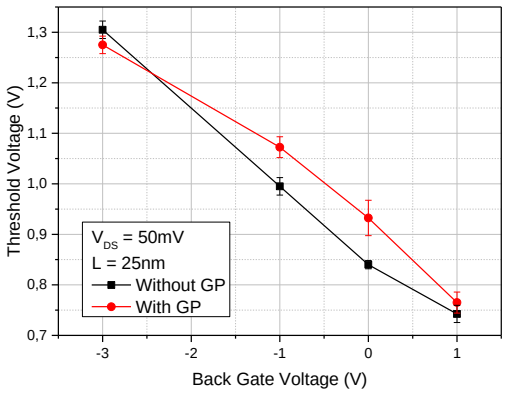

Fig. 5. Threshold voltage (V_T) as a function of back gate voltage for V_{DS} = 50mV and a channel length L = 25nm, with and without Ground Plane (GP).

The ground plane (GP) is a layer of high doping below the third interface (buried oxide/silicon substrate) and it has been showing positive results in planar structures [2][3]. In comparison with the natural silicon doping concentration in the devices, $p^+ \approx 10^{15}$ cm^{-3}, the GP layer has a doping concentration $p^+ \approx 10^{18}$ cm^{-3}. This increase of the Na_{sub}, then, reduces the V_{FB3} and increases the V_{T3} and Φ_{sub}, as we can see in the (1), (5) and (6) equations.

From (2), we have that the Φ_{sub} affects, by its turn, the back gate voltage and, consequently, the body effect. We can see the effect in the figure 4, where the threshold voltage as a function of the channel length changes with the application of ground plane, in comparison with the case without GP, due the variation of the back gate voltage by the Φ_{sub} term.

It is observed that the use of GP increases the threshold voltage values, which is in accordance with other works [2][3][4].

When we analyze the figure 5, between V_{GB} = 0V and V_{GB} = 1V, it is possible to see the effect of the (3) and (4) equations to the reduction of the third interface-depleted region, which was more detailed in [4]. This reduces the effect of Φ_{sub} over the threshold voltage, making it more linearized.

B. *Subthreshold Swing – SS*

Applying a FFT with five points smooth filter on the logarithm of the drain current; after, the first derivative in relation to V_G and, then, inverting the result and multiplying by 1000, we obtain the subthreshold swing SS in mV/decade.

Figure 6 represents the subthreshold swing as a function of the channel length with V_{GB} = 0V and V_{DS} = 50mV for two situations: device with ground plane and device without it.

By verifying the curves, it is noted that there is not a notable difference between the SS values with or without ground plane. But it is possible to note the strong short channel effects with the higher values for small L. This SCE is not observed in V_T curve.

C. *Drain-Induced Barrier Lowering – DIBL*

DIBL is the parameter that measurement the influence of the drain voltage over the threshold voltage. It is one of the short channel effects.

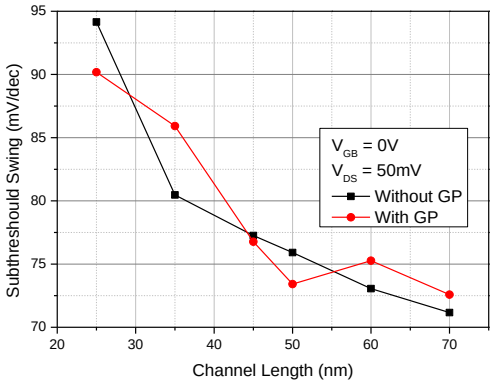

Fig. 6. Subthreshold Swing (SS) as a function of the channel length (L) for V_{DS} = 50mV and V_{GB} = 0V, with and without Ground Plane.

From the threshold voltage (V_{Ttri}), the drain current in triode related with it was taken. With that, the same value in the saturation current was sought, using linear interpolation if necessary. Lastly, from that current value, the gate voltage that is related with it was taken; this is called saturation threshold voltage (V_{Tsat}). The DIBL is calculated by the equation (7).

$$DIBL = -\frac{V_{Tsat} - V_{Ttri}}{V_{DSsat} - V_{DStri}} \qquad (7)$$

Where V_{DSsat} is the drain-source voltage in saturation (V_{DS} = 1V) and V_{DStri} is the drain-source voltage in triode (V_{DS} = 50mV).

Figure 7 shows the drain-induced barrier lowering as a function of channel length with V_{GB} = 0V for two cases: device with ground plane and device without it.

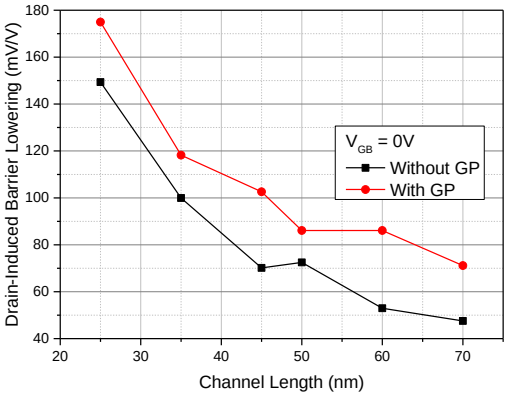

Fig. 7. Drain-induced barrier lowering (DIBL) as a function of the channel length (L) for V_{GB} = 0V, with and without Ground Plane.

DIBL in the device with ground plane has suffered an increase on its value in comparison with the one without it. This indicates that, to the measured devices, the use of that doping below the third interface impairs the charge control by the gate bias, intensifying the decreasing of drain barrier. And it is possible to note, again, the strong short channel effects with the higher values for small L.

Conclusion

The effect of ground plane (GP) on UTBB (Ultra-Thin Body and Buried oxide) SOI (Silicon-On-Insulator) MOSFET is experimentally analyzed for short channel devices (down to 25nm) in this paper. The GP typically improves the gate to channel electrostatic coupling. However, the short channel effects is observed for devices between 70 and 25nm of channel length on SS and DIBL and, for this last one, a clear improvement is observed for devices without Ground Plane (GP).

Acknowledgment

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